



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,273	09/10/2003	Robert A. Dunstan	110349-134509	5025

25943 7590 06/02/2006

SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITE 1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER

SCHELL, JOSEPH O

ART UNIT	PAPER NUMBER
----------	--------------

2114

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/660,273	Applicant(s) DUNSTAN ET AL.	
	Examiner Joseph Schell	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

Claims 1-40 have been examined.

Claims 1-40 have been rejected.

Claim Objections

1. The claims are objected to for the following informalities:

Claim 16 line 9 should say something like "wherein the BIOS performs the steps of" as the method steps are system characteristics of the BIOS as is implied by the use of "including."

Claim 32 lines 2 and 3 should read "the persistent storage **does not comprise a** valid..."

Claim 34 line 7 is objected to for the same reason as claim 16.

Claim 38 line 10 should read "**mark** the valid saved..."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Art Unit: 2114

2. Claims 13-15, 30-32 and 38-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Kohno (US Patent 6,523,125).

3. As per claim 13, Kohno ('125) discloses in an apparatus, a method of operation comprising:

a basic input/output system (BIOS) commencing a cold start reset process on re-application of AC power to the apparatus while the apparatus is in an un-powered state (column 19 lines 6-11);

the BIOS determining as part of the cold start reset process, whether a persistent storage of the apparatus comprises a valid saved operational state of the apparatus (column 19 lines 25-30, the signature is checked for);

the BIOS re-marking the valid saved operational state of the apparatus as invalid, if the persistent storage is determined to have a valid saved operational state of the apparatus (column 19 lines 41-51 and column 19 line 65 through column 20 line 1, the signature is disabled if the system settings are incorrect); and

the BIOS initiating a plurality of data transfer operations to transfer the saved operational state of the apparatus from the persistent storage to a memory of the apparatus to restore the saved operational state of the apparatus from the persistent storage to a memory of the apparatus (column 20 lines 10-12. While this is one by a routine stored in special SMM memory (column 12 lines 35-40), it can also be done by BIOS. See column 5 lines 10-13).

4. As per claim 14, Kohno ('125) discloses the method of claim 13, wherein the method further comprises on completion of the data transfer operations, the BIOS setting up an immediate wake event to immediately wake the apparatus, and placing the apparatus in a suspended to memory state, resulting in the set up immediate wake event to immediately wake the apparatus to cause the cold start reset process to be continued as a resume process, eventually leading to the apparatus to start operation in an active state, continuing from the restored operational state of the apparatus (column 19 lines 25-30, the signature designates that the system was hibernating which then allows the system to restore its prior state and resume operating).

5. As per claim 15, Kohno ('125) discloses the method of claim 13, wherein the method further comprises continuing with the cold start reset process, upon determining the persistent storage not comprising a valid saved operational state of the apparatus (column 20 lines 1-3, the user guides the system through its modified recovery).

6. As per claim 30, Kohno ('125) discloses a system comprising:

a memory (column 7 lines 1-3);

a persistent storage to store at least a saved operational state of the system (column 9 lines 43-45); and

a basic I/O system (BIOS) equipped to be operationally coupled to the memory and the persistent storage, to determine, as part of a cold start reset process commenced in response to re-application of AC power to the system while the system is

Art Unit: 2114

in an un-powered state (column 19 lines 6-11), whether the persistent storage comprises a valid saved operational state of the system (column 19 lines 25-30, the signature is checked for), and

to mark the valid saved operational state of the system as invalid upon determining existence of the valid saved operational state of the system in the persistent storage, before or substantially concurrent with commencing restoration of the saved operational state of the system from the persistent storage to the memory (column 19 lines 41-51 and column 19 line 65 through column 20 line 1, the signature is disabled if the system settings are incorrect).

7. As per claim 31, Kohno ('125) discloses the system of claim 30, where the BIOS is further equipped to initiate a plurality of data transfer operations to restore the saved operational state of the system from the persistent storage to the memory (column 20 lines 10-12. While this is one by a routine stored in special SMM memory (column 12 lines 35-40), it can also be done by BIOS. See column 5 lines 10-13), and

on completion of the data transfer operations, set up a wake event to wake the system, and place the system in a suspended to memory state, resulting in the set up wake event to immediately wake the system to cause the cold start reset process to continue as a resume process, eventually leading to the system to start operation in an active state, continuing from the restored operational state of the system (column 19 lines 25-30, the signature designates that the system was hibernating which then allows the system to restore its prior state and resume operating).

8. As per claim 32, Kohno ('125) discloses the system of claim 30, wherein the BIOS is further designed to continue the cold start reset process, upon determining the persistent storage not comprising a valid saved operational state of the system (column 20 lines 1-3, the user guides the system through its recovery in the event of an invalid saved state).

9. As per claim 38, Kohno ('125) discloses an article of manufacture comprising:
a storage medium (column 9 lines 43-45);
a plurality of programming instructions stored therein, implementing a basic I/O system (BIOS) equipped to

determine as part of a cold start reset process of an apparatus initiated in response to re-application of AC to the apparatus while the apparatus is in an un-powered state, whether a persistent storage of the apparatus comprises a valid saved operational state of the apparatus (column 19 lines 25-30, the signature is checked for), and

marking the valid saved operational state of the apparatus as invalid before or substantially concurrent with commencing restoration of the saved operational state of the apparatus from the persistent storage to a memory of the apparatus (column 19 lines 41-51 and column 19 line 65 through column 20 line 1, the signature is disabled if the system settings are incorrect).

Art Unit: 2114

10. As per claim 39, Kohno ('125) discloses the article of claim 38, where the BIOS is further equipped to initiate a plurality of data transfer operations to restore the saved operational state of the system from the persistent storage to the memory, and on completion of the data transfer operations, set up a wake event to wake the system, and place the system in a suspended to memory state, resulting in the set up wake event to immediately wake the system to cause the cold start reset process to continue as a resume process, eventually leading to the system to start operation in an active state, continuing from the restored operational state of the system (column 19 lines 25-30, the signature designates that the system was hibernating which then allows the system to restore its prior state and resume operating).

11. As per claim 40, Kohno ('125) discloses the article of claim 38, wherein the BIOS are further designed to continue and complete the cold start and reset process, after the persistent storage is determined not to comprise a saved operational state of the apparatus (column 20 lines 1-3, the user guides the system through its recovery in the event of an invalid saved state).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 1-2, 5-12, 16-17, 20-27, 29 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima (US Patent 5,875,120) in view of Thomas (US Patent 6,601,181).

13. As per claim 1, Matsushima ('120) discloses in an apparatus, a method of operation comprising:

the BIOS initiating as part of the intervention, a plurality of data transfer operations to transfer at least selected contents in a memory of the apparatus to a persistent store to save a persistent copy of an operational state of the apparatus (column 2 lines 1-8);

the BIOS further checking as part of the intervention, one or more times to determine whether the data transfer operations are completed (column 5 lines 46-57, after each sector is transferred, a status register is checked by BIOS to confirm the transfer); and

the BIOS further causing as part of the intervention, at least a processor of the apparatus to operate in a reduced power consumption mode in at least one time period while the BIOS is not performing said checking (column 7 lines 58-62).

Matsushima ('120) does not explicitly disclose the method wherein the suspend process is initiated in response to an AC failure.

Thomas ('181) teaches a system that stores the system's state to memory when AC power is removed and the system switches to battery power (column 6 lines 38-44).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) such that it prepares to hibernate upon the removal of AC power. This modification would have been obvious because data may be lost or corrupted and operations lost if power fails (Thomas ('181) column 1 lines 18-20) while going into a standby mode allows the system to prolong its battery life (Thomas ('181) column 6 lines 48-56).

14. As per claim 2, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 1, wherein said causing of at least a processor of the apparatus to operate in a reduced power consumption mode for at least one time period while the BIOS is not performing said checking, comprises the BIOS causing a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking

(Matsushima ('120) column 7 lines 58-62, multiple sectors are transferred and besides checking after each sector (and before the next sector), the CPU remains halted).

15. As per claim 5, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 2, wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, is performed after the BIOS initiated the data transfer operations (Matsushima ('120) column 7 lines 58-62, multiple sectors are transferred and besides checking after each sector (and before the next sector), the CPU remains halted).

16. As per claim 6, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 2, wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, is performed after the BIOS determined as part of a checking that the data transfer operations are still in progress (Matsushima ('120) column 5 lines 46-51, each sector of data is checked, with processor halting while waiting for the next transfer completion).

17. As per claim 7, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 2, wherein said causing of at least a processor of the apparatus to operate in a reduced power consumption mode for at least one time period while the BIOS is not performing said checking, further comprises the BIOS setting a timer to expire at the end of the first time period to interrupt the processor, causing the processor to exit the

Art Unit: 2114

reduced power consumption mode of operation (Matsushima ('120) column 12 lines 38-42).

18. As per claim 8, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 1, wherein said checking comprises the BIOS checking a plurality of times to determine whether the data transfer operations are completed (Matsushima ('120) column 12 lines 63-67, multiple sectors are transferred with a handshaking status reading performed by the BIOS for each transfer).

19. As per claim 9, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 1, wherein said causing comprises the BIOS causing at least a processor of the apparatus to operate in a reduced power consumption mode in a plurality of time periods while the BIOS is not performing said checking (Matsushima ('120) column 7 lines 58-62).

20. As per claim 10, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 1, wherein the method further comprises the BIOS marking the persistent copy of the operational state of the apparatus as valid, upon completion of the data transfer operations (Matsushima ('120) column 5 lines 26-43, the status register is marked by the HDD at the end of transactions initiated by the BIOS).

21. As per claim 11, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 1, wherein the method further comprises the BIOS configuring as part of the intervention, one or more wake events as ineligible to wake the apparatus after the apparatus enters the suspended to memory state, leaving AC re-availability as the only wake event eligible to wake the apparatus from the suspended to memory state (Thomas ('181) column 7 lines 17-18. It would be advantageous to further modify the system disclosed by Matsushima ('120) such that AC re-availability is the only valid restart event because it would prevent possible data loss, see Thomas ('181) column 7 lines 18-34).

22. As per claim 12, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 1, wherein the method further comprises the BIOS causing the suspend process to be completed subsequent to the completion of the data transfer operations (Thomas ('181) column 6 lines 48-56 teach that a suspend to disk operation allows the system state to be preserved in the event of a complete loss of power).

23. As per claim 16, Matsushima ('120) discloses a system comprising:

- a memory to store at least a current operational state of the system (Figure 1A element 15);
- a persistent storage (Figure 1A element 21);
- a processor (Figure 1A element 11);

and a basic I/O system (BIOS) operatively coupled to the memory , the persistent storage and the processor (column 9 line 67 through column 10 line 3), to save a persistent copy of the operational state of the system in the persistent storage, including

initiating a plurality of data transfer operations to copy the operational state into the persistent storage (column 12 lines 63-67);

checking as part of the intervention, one or more times to determine whether the data transfer operations are completed (column 7 lines 48-58. the handshaking is performed for each sector transferred), and

causing as part of the intervention, at least the processor to operate in a reduced power consumption mode in at least one time period while the BIOS is not performing said checking (column 7 lines 58-62).

Matsushima ('120) does not explicitly disclose the method wherein the suspend process is initiated in response to an AC failure.

Thomas ('181) teaches a system that stores the system's state to memory when AC power is removed and the system switches to battery power (column 6 lines 38-44).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) such that it prepares to hibernate upon the removal of AC power. This modification would have been obvious because data may be lost or corrupted and operations lost if power fails (Thomas ('181) column 1

lines 18-20) while going into a standby mode allows the system to prolong its battery life (Thomas ('181) column 6 lines 48-56).

24. As per claim 17, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16, wherein the BIOS causes at least the processor to operate in a reduced power consumption mode for at least one time period while the BIOS is not performing said checking, by causing the processor to be at least halted for a first time period while the BIOS is not performing said checking (Matsushima ('120) column 7 lines 58-62, multiple sectors are transferred and besides checking after each sector (and before the next sector), the CPU remains halted).

25. As per claim 20, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 17, wherein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, after the BIOS initiated the data transfer operations Matsushima ('120) column 7 lines 58-62, multiple sectors are transferred and besides checking after each sector (and before the next sector), the CPU remains halted).

26. As per claim 21, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 17, wherein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, after the BIOS determined as part of a checking that the data transfer operations are still in progress

(Matsushima ('120) column 5 lines 46-51, each sector of data is checked, with processor halting while waiting for the next transfer completion).

27. As per claim 22, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 17, wherein the BIOS causes at least the processor to operate in a reduced power consumption mode for at least one time period while the BIOS is not performing said checking, by further setting a timer to expire at the end of the first time period to interrupt the processor, causing the processor to exit the reduced power consumption mode of operation (Matsushima ('120) column 12 lines 38-42).

28. As per claim 23, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16, wherein the BIOS checks to determine whether the data transfer operations are completed a plurality of times (Matsushima ('120) column 12 lines 63-67; multiple sectors are transferred with a handshaking status reading performed by the BIOS for each transfer).

29. As per claim 24, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16, wherein the BIOS causes at least a processor of the apparatus to operate in a reduced power consumption mode while the BIOS is not performing said checking, in a plurality of time periods (Matsushima ('120) column 7 lines 58-62, the CPU is halted while each sector is transferring).

Art Unit: 2114

30. As per claim 25, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16, wherein the BIOS further marks the saved copy of the operational state of the apparatus as valid, upon completion of the data transfer operations (Matsushima ('120) column 5 lines 26-43, the status register is marked by the HDD at the end of transactions initiated by the BIOS).

31. As per claim 26, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16, wherein the BIOS further configures as part of the intervention, one or more wake events as ineligible to wake the apparatus after the apparatus enters the suspended to memory state, leaving AC re-availability as the only wake event eligible to wake the apparatus from the suspended to memory state (Thomas ('181) column 7 lines 17-18. It would be advantageous to further modify the system disclosed by Matsushima ('120) such that AC re-availability is the only valid restart event because it would prevent possible data loss, see Thomas ('181) column 7 lines 18-34).

32. As per claim 27, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16, wherein the BIOS further causes the suspend process to be completed subsequent to the completion of the data transfer operations (Thomas ('181) column 6 lines 48-56 teach that a suspend to disk operation allows the system state to be preserved in the event of a complete loss of power).

Art Unit: 2114

33. As per claim 29, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16, wherein the system is a selected one of a set-top box, an entertainment control console, a video recorder, and a video player (Matsushima ('120) Figure 1A, element 19).

34. As per claim 34, Matsushima ('120) discloses an article of manufacture comprising:

a storage medium (Figure 1A element 21); and

a plurality of programming instructions stored therein, implementing a basic I/O system (BIOS) to suspend the apparatus hosting the BIOS to a suspended to memory state, and save a persistent copy of an operational state of the apparatus (column 2 lines 1-8), including initiating a plurality of data transfer operations to transfer at least selected contents of a memory of the apparatus to a persistent storage of the apparatus (column 11 line 66 through column 12 line 3);

checking as part of the intervention, one or more times to determine whether the data transfer operations are completed (column 5 lines 46-57, after each sector is transferred, a status register is checked by BIOS to confirm the transfer), and causing as part of the intervention, at least a processor of the apparatus to operate in a reduced power consumption mode in at least one time period while the BIOS is not performing said checking (column 7 lines 58-62).

Matsushima ('120) does not explicitly disclose the method wherein the suspend process is initiated in response to an AC failure.

Thomas ('181) teaches a system that stores the system's state to memory when AC power is removed and the system switches to battery power (column 6 lines 38-44).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) such that it prepares to hibernate upon the removal of AC power. This modification would have been obvious because data may be lost or corrupted and operations lost if power fails (Thomas ('181) column 1 lines 18-20) while going into a standby mode allows the system to prolong its battery life (Thomas ('181) column 6 lines 48-56).

35. As per claim 35, Matsushima ('120) in view of Thomas ('181) discloses the article of claim 34, wherein the BIOS is further equipped to mark the persistent copy of the operational state of the apparatus as valid, upon completion of the data transfer operations (Matsushima ('120) column 5 lines 26-43, the status register is marked by the HDD at the end of transactions initiated by the BIOS).

36. As per claim 36, Matsushima ('120) in view of Thomas ('181) discloses the article of claim 34, wherein the BIOS is further equipped to configure as part of the intervention, one or more wake events as ineligible to wake the apparatus after the

apparatus enters the suspended to memory state, leaving AC re-availability as the only wake event eligible to wake the apparatus from the suspended to memory state (Thomas ('181) column 7 lines 17-18. It would be advantageous to further modify the system disclosed by Matsushima ('120) such that AC re-availability is the only valid restart event because it would prevent possible data loss, see Thomas ('181) column 7 lines 18-34).

37. As per claim 37, Matsushima ('120) in view of Thomas ('181) discloses the article of claim 34, wherein the BIOS is further equipped to cause the suspend process to be completed subsequent to the completion of the data transfer operations (Thomas ('181) column 6 lines 48-56 teach that a suspend to disk operation allows the system state to be preserved in the event of a complete loss of power).

38. Claims 3-4 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima ('120) in view of Thomas ('181) and in further view of Mustafa (US Patent 6,243,831).

39. As per claim 3, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 2. Matsushima ('120) in view of Thomas ('181) does not expressly disclose the method wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, comprises the BIOS

causing a processor of the apparatus to enter an ACPI C1 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) in view of Thomas ('181) such that it utilizes the ACPI specification. This modification would have been obvious because it provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to put the system into an ACPI S1 state when waiting for HDD IO. This modification would have been obvious because S1 allows the processor to be turned off, while having very little performance degradation upon returning to normal operation (Mustafa ('831) column 5 lines 53-65).

40. As per claim 4, Matsushima ('120) in view of Thomas ('181) discloses the method of claim 2. Matsushima ('120) in view of Thomas ('181) does not expressly disclose the

Art Unit: 2114

method wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, comprises the BIOS causing a processor of the apparatus to enter a selected one of an ACPI C2 state and an ACPI C3 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) in view of Thomas ('181) such that it utilizes the ACPI specification. This modification would have been obvious because it provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to allow the system to select between ACPI C2 and ACPI C3 states when not performing checking. This modification would have been obvious because ACPI C2 provides more power savings than C1, with slight performance degradation upon resuming normal operation (Mustafa ('831) column 5

lines 59-65), while S3 provides even greater power saving with further degraded performance upon resuming normal operation (Mustafa ('831) column 5 line 66 through column 6 line 5). The BIOS has a list of available sleep states (Mustafa ('831) column 6 lines 26-29), and the time that the processor will be in standby mode varies depending on the transaction (Matsushima ('120) column 7 lines 27-30, the expected frequency of interrupts will vary depending on devices being managed and their needs).

41. As per claim 18, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 17. Matsushima ('120) in view of Thomas ('181) does not explicitly disclose the system wherein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, by causing the processor to enter an ACPI C1 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) in view of Thomas ('181) such that it utilizes the ACPI specification. This modification would have been obvious because it

Art Unit: 2114

provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to put the system into an ACPI S1 state when waiting for HDD IO. This modification would have been obvious because S1 allows the processor to be turned off, while having very little performance degradation upon returning to normal operation (Mustafa ('831) column 5 lines 53-65).

42. As per claim 19, Matsushima ('120) in view of Thomas ('181) discloses the system of claim 17. Matsushima ('120) in view of Thomas ('181) does not explicitly disclose the system herein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, by causing the processor to enter a selected one of an ACPI C2 state and an ACPI C3 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) in view of Thomas ('181) such that it utilizes the ACPI specification. This modification would have been obvious because it provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to allow the system to select between ACPI C2 and ACPI C3 states when not performing checking. This modification would have been obvious because ACPI C2 provides more power savings than C1, with slight performance degradation upon resuming normal operation (Mustafa ('831) column 5 lines 59-65), while S3 provides even greater power saving with further degraded performance upon resuming normal operation (Mustafa ('831) column 5 line 66 through column 6 line 5). The BIOS has a list of available sleep states (Mustafa ('831) column 6 lines 26-29), and the time that the processor will be in standby mode varies depending on the transaction (Matsushima ('120) column 7 lines 27-30, the expected frequency of interrupts will vary depending on devices being managed and their needs).

43. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima ('120) in view of Thomas ('181) as applied to claim 16, and in further view of Sadashivaiah (US Patent 5,638,541).

Matsushima ('120) in view of Thomas ('181) discloses the system of claim 16.

Matsushima ('120) in view of Thomas ('181) does not expressly disclose the system further comprising a networking interface operatively coupled to the BIOS.

Sadashivaiah ('541) teaches a power management driver that intercepts power down requests and reissues them to the BIOS such that it can micromanage which devices are placed in standby mode (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) in view of Thomas ('181) such that it uses a power management driver as a BIOS interface for standby and wakeup events. This modification would have been obvious because it would allow the system to periodically wake and service network queries and maintain a network connection while otherwise maintaining a standby state (Sadashivaiah ('541) column 5 line 64 through column 6 line 45).

44. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohno ('125) in view of Sadashivaiah ('541).

Kohno ('125) discloses the system of claim 30. Kohno ('125) does not expressly disclose the system wherein the system further comprises a networking interface operatively coupled to the BIOS.

Sadashivaiah ('541) teaches a power management driver that intercepts power down requests and reissues them to the BIOS such that it can micromanage which devices are placed in standby mode (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Matsushima ('120) in view of Thomas ('181) such that it uses a power management driver as a BIOS interface for standby and wakeup events. This modification would have been obvious because it would allow the system to periodically wake and service network queries and maintain a network connection while otherwise maintaining a standby state (Sadashivaiah ('541) column 5 line 64 through column 6 line 45).

Conclusion

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Watanabe ('266) and Nguyen ('059) teach systems that use the BIOS to put a processor to sleep while it waits for IO, Nakamura ('931) teaches a system wherein upon detection of a power failure the BIOS employ a DMA controller to transfer memory contents to storage, and Govindaraj ('298) teaches a system that saves data on power failure and checked for corruption before restoring.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS


SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER